## REMARKS/ARGUMENTS

In the Official Action, the Examiner rejected Claims 1-6 under 35 U.S.C. § 103(a), as being unpatentable over Bogholtz et al., U.S. Patent 5,195,097 in view of Jung et al., U.S. Patent 6,067,255.

Before discussing the prior art relied upon by the Examiner, it is very beneficial to first briefly review the structure of the invention of the subject application. The invention of the subject application is directed to a method for testing memories with seamless data input/output by interleaving seamless bank commands. According to the method, **both the seamless data input/output (DQ) as well as seamless control commands (CLK, Bank #0~#3)** are applied on the memories to be tested so as to easily detect the weakened memories.

With reference to Figs. 9 and 10A admitted by the applicant in the referenced application, the prior testing method provides **only** the **seamless data input/output (DQ)** to test the memories. It is noted that the control pins of these memories still do not receive seamless control commands. In other words, such conventional operations made to the memories are not sufficient to detect weakened memory cells.

In contradistinction, the Bogholtz et al. reference is directed to a method that continuously provides test data to a memory from a multiplexer during repetitions of a test loop and when new test loops are introduced, with no intervals in the test data. However, the reference does not suggest to supply seamless control commands to the control pins of the memories, as claimed in the present invention. Quite obviously, the technique taught by Bogholtz et al. is the same as the prior art shown in Figs. 9 and 10 and its drawbacks are intended to be overcome by the present invention.

With reference to another cited U.S. Patent, 6,067,255, Jung et al. discloses a merged memory and logic (MML) IC. When reviewing the '255, Jung et al. indicate that the conventional

SDRAM architecture only has one row address strobe signal RAS, one column address strobe signal CAS and one write enable signal WE as shown in Fig. 1. Such an SDRAM architecture, however, is unsuitable for testing the MML IC (see column 1 line 66 to column 2 line 16). In order to provide a memory controlling system and methods for MML integration, Jung et al. proposed a new MML architecture as shown in Fig. 3 having a dual row address strobe signals RASa, RASb, dual column address strobe signals CASa, CASb and dual write enable signals WEa, WEb.

The timing diagram of a read operation of a memory block of MML IC proposed by Jung et al. is depicted in Fig. 4. In one clock, for example T2, two commands "Read" for bank A, and "Row Active" for bank B exist simultaneously thus allowing test data to be supplied to the memory banks seamlessly. However, with respect to control commands applied to the memory banks, these control commands are not seamlessly presented. In short, there are intervals existing among the control commands.

Further, the Examiner rejected Claims 7-15 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention.

To overcome the rejection made to claims 7-15, applicant cancels claims 7-15 and writes new separate independent claims 16 and 19 using the subject matter of page 7 lines 14-17 of the present specification without introducing any new matter.

After the foregoing amendments, it is believed that the present invention is patentable in view of the cited prior art, thus, an early granting of the application is respectfully requested.

The Applicant asks the Examiner to reconsider the claims and issue a Notice of Allowance.

The U.S. Patent and Trademark Office is hereby authorized to charge any fees, if any, or discrepancies in fees required, to Deposit Account **07-2400**.

Respectfully submitted,
JACKSON WALKER L.L.P.

Thomas E. Sisson, Reg. No. 29,348
112 E. Pecan Street, Suite 2100
San Antonio, Texas 78205
Phone: (210) 978-7700
Fax: (210) 978-7790
Attorneys for Applicant

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